Data Sheet
February 1992

AT&T Microelectronics

T7281 Adaptive Differential Pulse-Code Modulation Transcoder

Features

- ADPCM coding and decoding with bypass processing
- μ-law and A-law 64 kbits/s PCM compatible
- ANSI and CCITT G.726 compatible at 40 kbits/s, 32 kbits/s, 24 kbits/s, and 16 kbits/s
- Variable-rate ADPCM, coding at 40 kbits/s, 32 kbits/s, 24 kbits/s, 16 kbits/s, and 8 kbits/s
- 16-channel implementation (M encoders and N decoders, where M + N = 16 channels)
- Independent feature control on a per-channel, 125 μs time-slot basis
- Reset of internal memory states under user control
- Pin-for-pin replacement for T7280

Description

The T7281 Adaptive Differential Pulse-Code Modulation (ADPCM) Transcoder is a single-chip integrated circuit that digitally reencodes 64 kbits/s PCM (8 kHz sampling) to ADPCM at various bit rates. The device provides 16 channels of encoding or decoding, any one of which can function as either an encoder or decoder, independent of the other channels. The T7281 is manufactured by using CMOS technology and is available in a 24-pin, plastic DIP or in a 44-pin, plastic, leaded chip carrier (PLCC).

Description (continued)

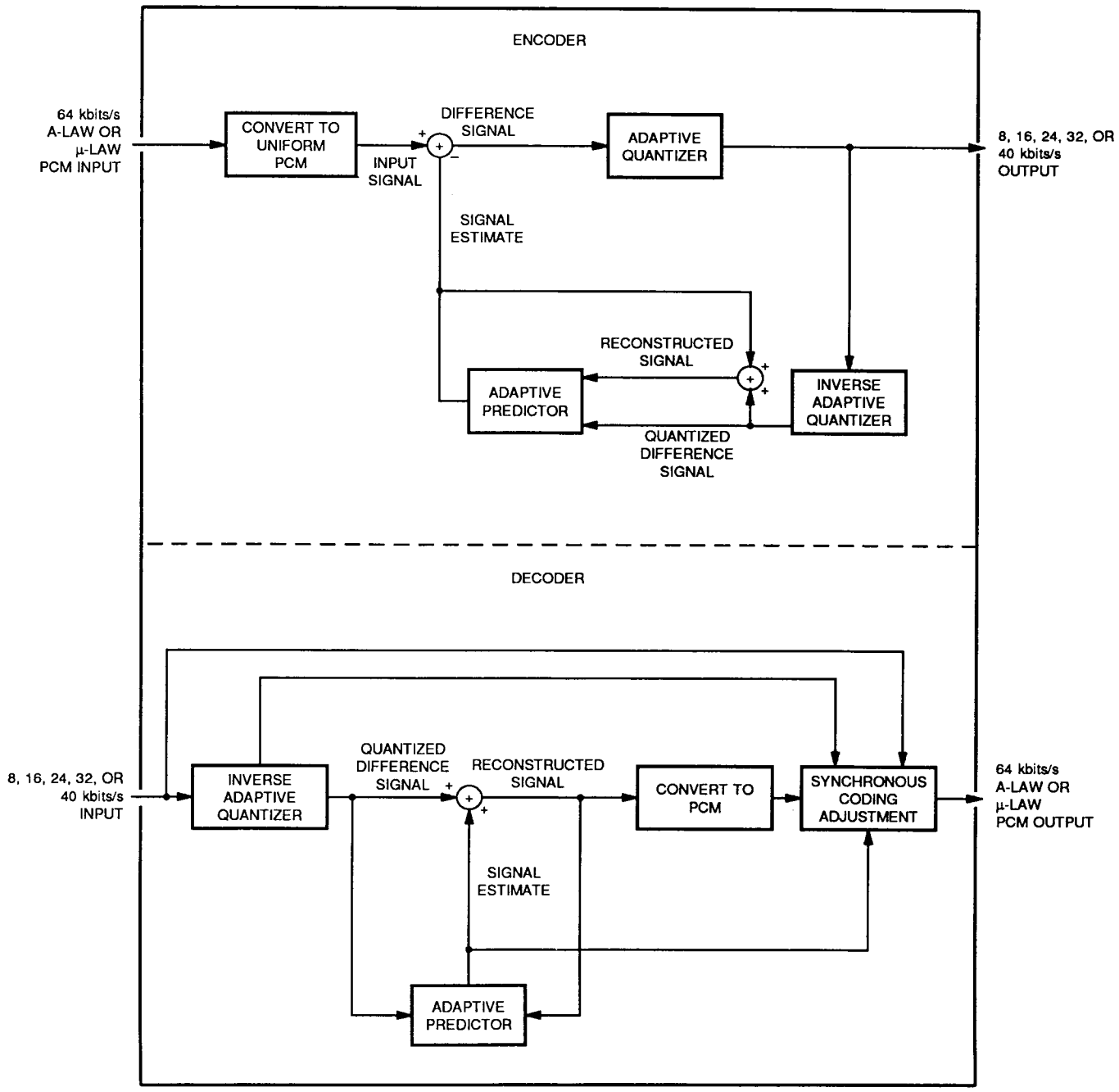


Figure 1. Block Diagram

Pin Information

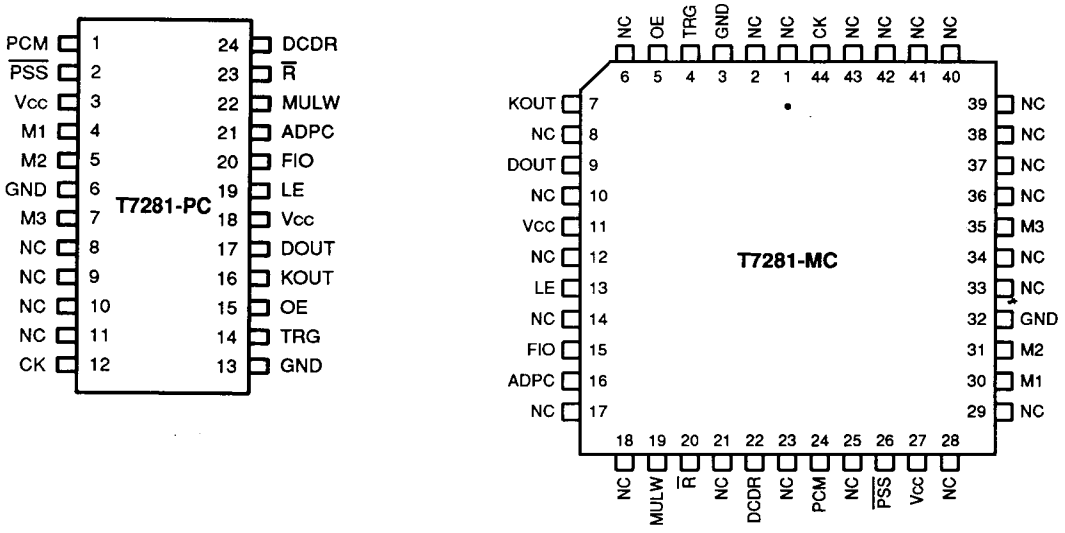


Figure 2. Pin Diagrams

Table 1. Pin Descriptions

DIP	PLCC	Symbol	Type	Name/Function
1	24	PCM	I	**PCM In.** Input to the encoder.
2	26	$\overline{PSS}$	I	**Passthrough Input to Output (Active-Low).** A low on this pin causes an 8-bit sample to pass through to the output (transparent to the user).
3, 18	11, 27	Vcc	I	**5 V Supply.**
4 5 7	30 31 35	M1 M2 M3	I	**ADPCM Quantizer Rate Select.** M1 M2 M3 Rate CCITT ANSI 1 0 1 40 kbits/s G.726 T1Y1/87-040 1 0 0 32 kbits/s G.726 T1.301-1987 0 0 0 24 kbits/s G.726 T1Y1/87-040 0 1 1 16 kbits/s G.726 — 0 1 0 8 kbits/s — — **Note:** Voice quality at 8 kbits/s is poor, so applications should be restricted to short (several 100 ms) intervals. System-level subjective testing is recommended.
6, 13	3, 32	GND	I	**Ground.**
8—11	1, 2, 6, 8, 10, 12, 14, 17, 18, 21, 23, 25, 28, 29, 33, 34, 36—43	NC	—	**No Connect.** Must be left floating.
12	44	CK	I	**4.096 MHz Clock.** 50% duty cycle.
14	4	TRG	I	**Channel Trigger.** 128 kHz sync pulse.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

DIP	PLCC	Symbol	Type	Name/Function
15	5	OE	I	**Output Enable.** A high on this pin enables both DOUT and KOUT outputs. A low on this pin configures both outputs into a high-impedance state.
16	7	KOUT	O	**Knocked Output.** 3-state output.
17	9	DOUT	O	**Standard Output.** 3-state output.
19	13	LE	I	**Input Latch Enable.** A high on this pin enables the input.
20	15	FIO	I	**4 MHz I/O.** A high on this pin allows 4 MHz data input/output operation; a low allows 2 MHz data input/output operation.
21	16	ADPC	I	**ADPCM In.** Input to decoder.
22	19	MULW	I	**μ-law Coding.** A high on this pin for μ-law and a low for A-law coding.
23	20	$\overline{R}$	I	**Channel Reset (Active-Low).** A low on this pin resets the channel.
24	22	DCDR	I	**Decoder.** A high on this pin enables the decoder; a low enables the encoder.

Functional Description

The T7281 ADPCM Transcoder operates at 4.096 MHz and provides 16 channels of encoding or decoding, i.e., M encoders and N decoders, where M + N = 16. All of the following modes can be enabled or changed on any one channel independent of the other channels. The modes controlled by the MULW, DCDR, $\overline{PSS}$, M1, M2, M3, and $\overline{R}$ pins can occur rapidly, even at the 128 kHz per channel rate, if desired.

μ-law/A-law

The user can specify the input and output PCM code words to be in either μ-law (MULW = 1) or A-law (MULW = 0) format in accordance with CCITT Recommendation G.711.

Encoder/Decoder

Each channel can operate as either an encoder or a decoder. If operating as an encoder (DCDR = 0), the PCM (pin 1) bits are read and encoded into an ADPCM word. If operating as a decoder (DCDR = 1), the ADPC (pin 21) bits are read and decoded into a PCM word.

Passthrough

Any channel can be set for no coding or passthrough ($\overline{PSS}$ = 0) such that the input 8-bit PCM sample is passed transparently to the output with a 512 bit delay (125 μs). If the channel is operating as an encoder (DCDR = 0), the PCM bits are passed through to the output. If the channel is operating as a decoder (DCDR = 1), the ADPC bits are passed through to the output.

Quantizer Control

Since mode changes can occur rapidly, the T7281 ADPCM Transcoder is ideal for variable-rate coding at rates of 40 kbits/s or less. The 16 kbits/s and 24 kbits/s rates decrease performance; however, a quality/bit-rate tradeoff is desirable in some applications. Voice quality at 8 kbits/s coding is poor, so its use should be restricted to short intervals (several 100 ms). Subjective testing at the system level is recommended.

Functional Description (continued)

Table 2. 5-, 4-, 3-, 2-, and 1-Bit Mapping from Decision Regions to I3, I2, I1, I0, and Ia

Decision Intervals	31 Level I3, I2, I1, I0, Ia	Decision Intervals	15 Level I3, I2, I1, I0, Ia	Decision Intervals	7 Level I3, I2, I1, I0, Ia	Decision Intervals	4 Level I3, I2, I1, I0, Ia	Decision Intervals	2 Level I3, I2, I1, I0, Ia
$[d_{15}, +\infty)$	01111	$[d_7, +\infty)$	0111X	$[d_3, +\infty)$	011XX	$[d_1, +\infty)$	01XXX	$(0, +\infty)$	0xxxx
$[d_{14}, d_{15})$	01110	—	—	—	—	—	—	—	—
$[d_{13}, d_{14})$	01101	$[d_6, d_7)$	0110X	—	—	—	—	—	—
$[d_{12}, d_{13})$	01100	—	—	—	—	—	—	—	—
$[d_{11}, d_{12})$	01011	$[d_5, d_6)$	0101X	$[d_2, d_3)$	010XX	—	—	—	—
$[d_{10}, d_{11})$	01010	—	—	—	—	—	—	—	—
$[d_9, d_{10})$	01001	$[d_4, d_5)$	0100X	—	—	—	—	—	—
$[d_8, d_9)$	01000	—	—	—	—	—	—	—	—
$[d_7, d_8)$	00111	$[d_3, d_4)$	0011X	$[d_1, d_2)$	001XX	$(0, d_1)$	00XXX	—	—
$[d_6, d_7)$	00110	—	—	—	—	—	—	—	—
$[d_5, d_6)$	00101	$[d_2, d_3)$	0010X	—	—	—	—	—	—
$[d_4, d_5)$	00100	—	—	—	—	—	—	—	—
$[d_3, d_4)$	00011	$[d_1, d_2)$	0001X	—	—	—	—	—	—
$[d_2, d_3)$	00010	—	—	—	—	—	—	—	—
$[d_1, d_2)$	00001	—	—	—	—	—	—	—	—
$[d_{-1}, d_1)$	11111	$[d_{-1}, d_1)$	1111X	$[d_{-1}, d_1)$	111XX	$[d_{-1}, 0)$	11XXX	—	—
$[d_{-2}, d_{-1})$	11110	—	—	—	—	—	—	—	—
$[d_{-3}, d_{-2})$	11101	$[d_{-2}, d_{-1})$	1110X	—	—	—	—	—	—
$[d_{-4}, d_{-3})$	11100	—	—	—	—	—	—	—	—
$[d_{-5}, d_{-4})$	11011	$[d_{-3}, d_{-2})$	1101X	$[d_{-2}, d_{-1})$	110XX	—	—	—	—
$[d_{-6}, d_{-5})$	11010	—	—	—	—	—	—	—	—
$[d_{-7}, d_{-6})$	11001	$[d_{-4}, d_{-3})$	1100X	—	—	—	—	—	—
$[d_{-8}, d_{-7})$	11000	—	—	—	—	—	—	—	—
$[d_{-9}, d_{-8})$	10111	$[d_{-5}, d_{-4})$	1011X	$[d_{-3}, d_{-2})$	101XX	$(-\infty, d_{-1})$	10XXX	—	—
$[d_{-10}, d_{-9})$	10110	—	—	—	—	—	—	—	—
$[d_{-11}, d_{-10})$	10101	$[d_{-6}, d_{-5})$	1010X	—	—	—	—	—	—
$[d_{-12}, d_{-11})$	10100	—	—	—	—	—	—	—	—
$[d_{-13}, d_{-12})$	10011	$[d_{-7}, d_{-6})$	1001X	$[d_{-\infty}, d_{-3})$	100XX	—	—	—	—
$[d_{-14}, d_{-13})$	10010	—	—	—	—	—	—	—	—
$[d_{-15}, d_{-14})$	10001	$[d_{-\infty}, d_{-7})$	1000X	—	—	—	—	—	—
$[d_{-\infty}, d_{-15})$	10000	—	—	—	—	—	—	$(0, -\infty)$	1xxxx

Note: x = don't care.

Channel Reset

The channel reset ($\overline{R}$ = 0) mode control bit initializes all of the state variables of any channel to known values. These values are specified in CCITT and ANSI specifications. Digital test vectors can then be applied at the input. A unique output vector can then be generated and compared to a reference output vector. Since each channel can be reset independently, it is possible to reset and test an unused channel without affecting the remaining channels. The reset can be thought of as an instantaneous reset. It should be asserted at the same time as the first valid data sample of a sequence. This causes the internal states to be initialized and followed by processing

Functional Description (continued)

Channel Reset (continued)

of the first data sample. If the reset is asserted on the sample prior to the first valid sample, the device processes and adapts on one undefined sample before processing the first valid sample.

PCM and ADPCM I/O

The T7281 ADPCM Transcoder uses serial data I/O. There are two input pins, PCM and ADPC, and two output pins, DOUT and KOUT.

Inputs

If the T7281 is operating as an encoder (DCDR = 0), data is read from the PCM pin. If it is operating as a decoder (DCDR = 1), data is read from the ADPC pin. Data is read most significant bit (MSB) first. For PCM, which has eight bits (s, a, b, c, w, x, y, and z), the s bit is the MSB. For ADPCM (I3, I2, I1, I0, Ia, Ib, Ic, and Id), the I3 bit is the most significant bit. Normally, there are a maximum of five significant bits, I3—Ia, with the Ib—Id bits being inconsequential. However, in the passthrough mode, all eight bits are passed through.

Separate pins are provided in case the PCM and ADPCM data streams come from separate sources. For many applications, these two pins can be tied together. Figure 3 provides an I/O functional description.

I/O Control

The 16-channel T7281 ADPCM Transcoder requires a 4.096 MHz clock (CK). Three timing definitions are used relative to this clock: frame, channel, and bit time slot. A frame is the time between samples of a standard 8 kHz PCM or ADPCM sequence and is 125 μs (512 clock cycles) long. A channel is defined as 32 clock cycles and contains the standard 8 kHz PCM or ADPCM sample. A bit time slot is 1 clock cycle and is defined relative to the TRG input (see Figure 4).

Transitions occur on all inputs and outputs on the positive-going edge of the 4.096 MHz clock. All inputs, except output enable (OE), are latched at the falling edge of the clock. The data on outputs DOUT and KOUT is guaranteed to be valid for one propagation delay, tCKHDOV, after the rising edge of the clock (see the Timing Characteristics section).

By having the output valid a short time after the rising edge and the input latched on the falling edge, it is possible to cascade transcoders without intermediate logic.

Outputs

The DOUT and KOUT pins are 3-stated outputs controlled by the OE pin. Data is available on DOUT one frame (512 clock cycles) after the input. This delay is maintained for all modes, including passthrough ($\overline{\text{PSS}}$ = 0). The data on KOUT (the knocked output) is identical to the data on DOUT except that it is available one channel (32 clock cycles) earlier, allowing the output data to be processed with a delay time of less than one frame.

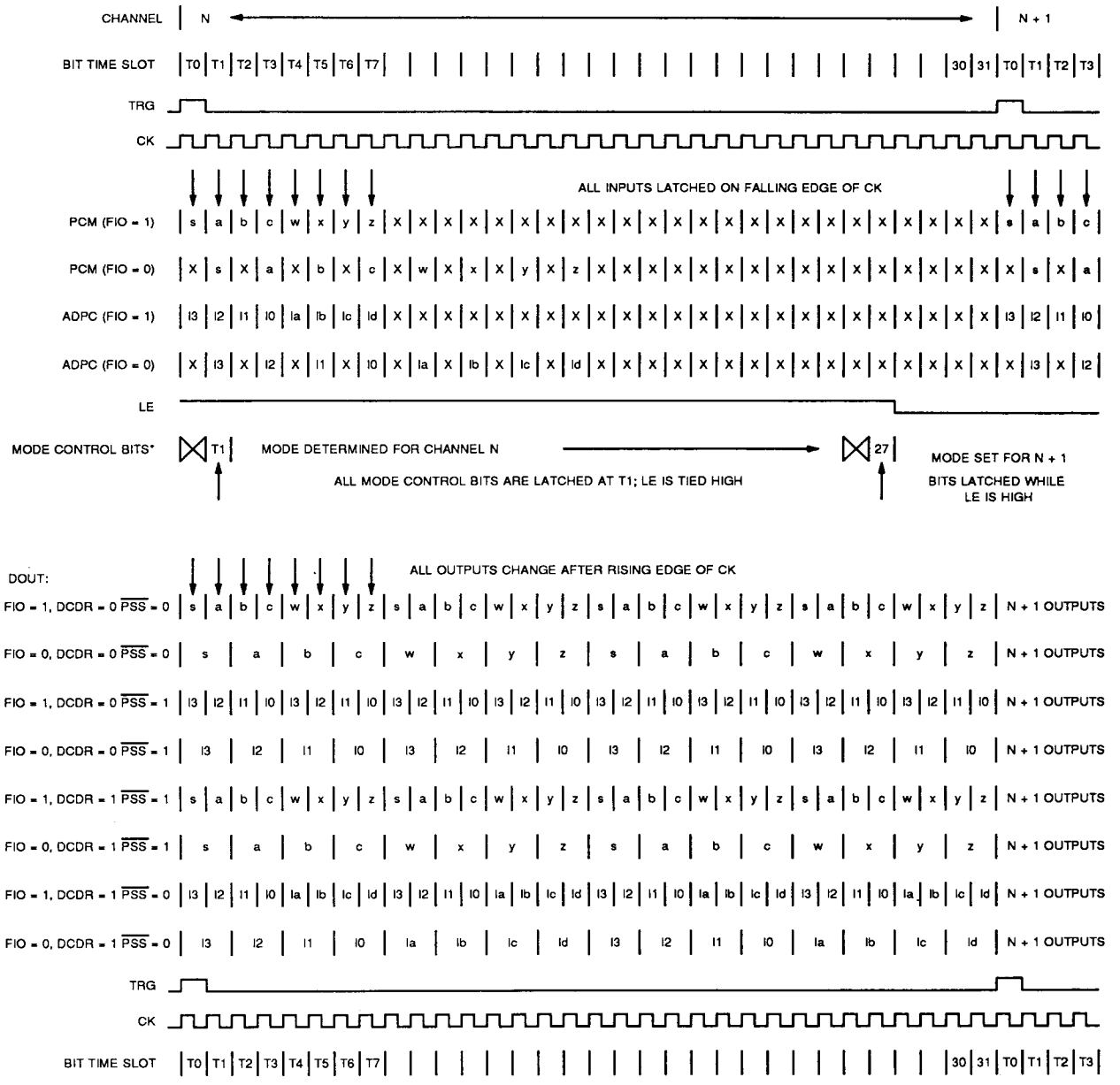
Since there are 32 clock cycles per channel and a maximum of 8 significant bits, the output is repeated (see Figure 3 for details). For 16, 24, and 32 kbits/s decoder operation without passthrough, the four most significant bits, I3, I2, I1, I0, are repeated within an 8-bit byte. For 40 kbits/s decoder operation without pass-through, the 8-bit byte, I3 I2 I1 I0 Ia 0 0 0, is repeated.

Fast and Slow I/O

The serial PCM and ADPCM inputs and outputs can be at either a 4.096 MHz data rate (FIO = 1) or a 2.048 MHz data rate (FIO = 0). The choice must be made for all channels. Figure 3 shows the bit alignment details for the two rates.

Functional Description (continued)

PCM and ADPCM I/O (continued)



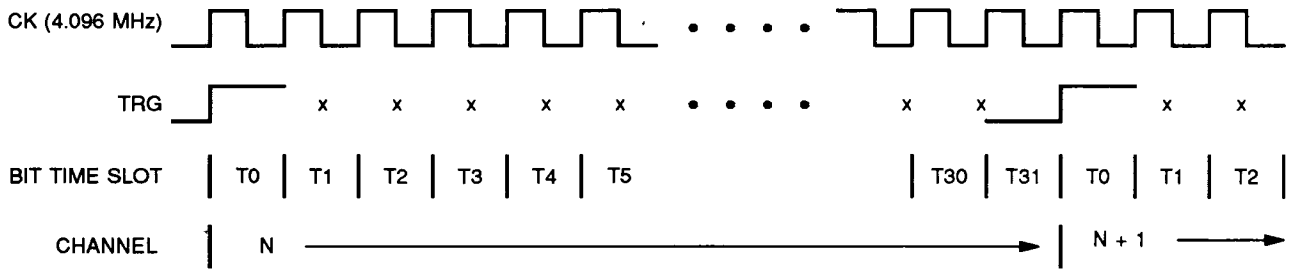
*The mode control bits are MULW, DCDR, $\overline{PSS}$, M1, M2, M3, and $\overline{R}$.

Notes:
x = don't care.
Ib, Ic, and Id on ADPC are inconsequential except in passthrough mode.
DOUT is delayed by one frame or 512 clock cycles from the input.
For 40 kbits/s decoder operation without passthrough, the 8-bit byte, |I3|I2|I1|I0|Ia|0|0|0|, is repeated in DOUT.

Figure 3. I/O Functional Description

Functional Description (continued)

PCM and ADPCM I/O (continued)



Note: x = don't care.

Figure 4. Bit Time Slot Definition

Channel Trigger

The channel trigger (TRG) is a 16 x 8 kHz channel-marking timing signal. The bit time slot (4.096 MHz clock period) in which TRG is first positive defines a sequence of bit time slots (T0, T1, . . . T31), as shown in Figure 4. Because of edge sensitivity, it does not matter how long TRG stays high. For example, TRG can be a pulse waveform up for 1 bit time slot and down for 31 bit time slots, or a square wave up for 16 bit time slots and down for 16 bit time slots. It is not even necessary that TRG repeat every 32 bit time slots. If another positive-going pulse is not received after 32 bit time slots, one is internally generated.

Input Latch Enable

The input latch enable (LE) allows the user to dictate when the control inputs are sampled. If LE is tied high, all control inputs for each channel are sampled at T1 time, which should be adequate for most applications. Otherwise, LE enables an input latch, the output of which is latched at T2 to actually configure the device. Thus, the control inputs are read each bit time slot that LE is high. The control used for channel N is the last latched control input between bit time slot 2 of channel N − 1 and bit time slot 1 of channel N, inclusive. Figure 3 shows an example in which LE is brought low at bit time slot 28, setting the mode for channel N + 1 based on the mode-control input states at bit time slot 27.

Output Enable

The output enable (OE) is the only unclocked input and controls the 3-state enabling for the two data outputs, DOUT and KOUT.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here is obtained by using these circuit parameters:

Human-Body Model ESD Threshold	
Device	**Voltage**
T7281-PC	>500 V
T7281-MC	>500 V

Absolute Maximum Ratings

Stress in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage	V_{DD}	−0.5	6.5	V
Power Dissipation	P_{dis}	—	600	mW
Storage Temperature	T_{stg}	−55	125	°C

Electrical Characteristics

Table 3. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Input Voltage					
Low	V_{IL}	—	GND	0.8	V
High	V_{IH}	—	2.2	V_{CC}	V
Output Voltage					
Low	V_{OL}	at 1.8 mA	GND	0.4	V
High	V_{OH}	at −2.2 mA	2.4	V_{CC}	V
Input Leakage Current					
Pin 12 (CK)	I_I	at 5 V	—	20	μA
All Other Input Pins	I_I	at 5 V	10	100	μA

Table 4. Operating Conditions

0 °C ≤ T_A ≤ 70 °C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Power Dissipation	P_{dis}	190	285	400	mW

Electrical Characteristics (continued)

ac Characteristics

Timing measurements (except propagation delays) are taken to and from a low reference point of 0.8 V and a high reference point of 2.2 V. The voltage swing through this range should start outside and pass through the range, such that the rise or fall is linear between 0.8 V and 2.2 V.

Propagation delay is generally measured from the 50% point of the reference signal transition to the 50% point of the output signal transition (see Figure 5).

The clock input is a TTL compatible signal that is internally buffered. The clock signal must conform to minimum and maximum pulse-width times.

All inputs are latched at the falling edge of the clock except output enable (OE). OE is an unclocked input and controls 3-state enabling for the two data outputs, DOUT and KOUT. These two outputs are guaranteed to be valid after a propagation delay, tCKHDOV, measured from the rising edge of the clock.

Timing Characteristics

Table 5. Clock Timing (See Figure 5.)

Symbol	Parameter	Min	Typ	Max	Unit
tCKHCKH	Clock Cycle Time	231.8	244	256.2	ns
tCKLCKH	Clock Low Time	95	122	147	ns
tCKHCKL	Clock High Time	97	122	149	ns
tr	Clock Rise Time	—	—	20	ns
tf	Clock Fall Time	—	—	20	ns

Table 6. Input Clock Timing (See Figure 5.)

Symbol	Parameter	Min	Typ	Max	Unit
tIXIV	Input Rise Time	—	—	20	ns
tIVIX	Input Fall Time	—	—	20	ns
tIVCKL	Input Valid to CK Low (Setup Time)	20	—	—	ns
tCKLIX	CK Low to Input Invalid (Hold Time)	20	—	—	ns

Table 7. Output Clock Timing (See Figure 5.)

C_L = 15 pF

Symbol	Parameter	Min	Typ	Max	Unit
tCKHDOV	CK High to DOUT, KOUT Valid	—	—	65	ns
tOVOV	Output Rise/Fall Time*	—	—	27.15	ns

* The result is measured at 4.8 V and 125 °C junction temperature with 15 pF capacitive loading.

Timing Characteristics (continued)

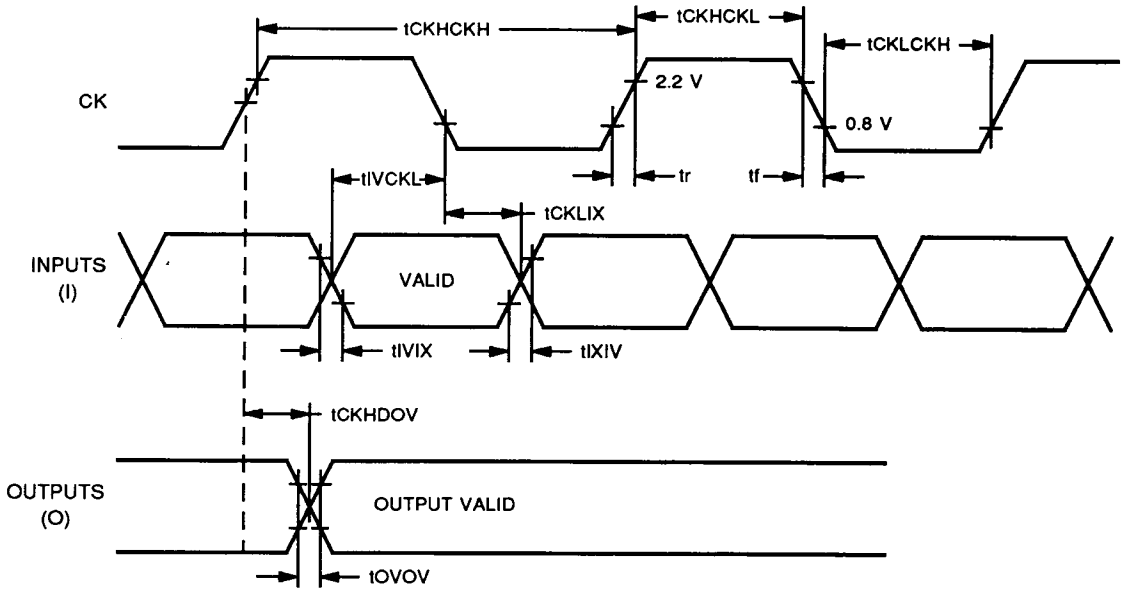
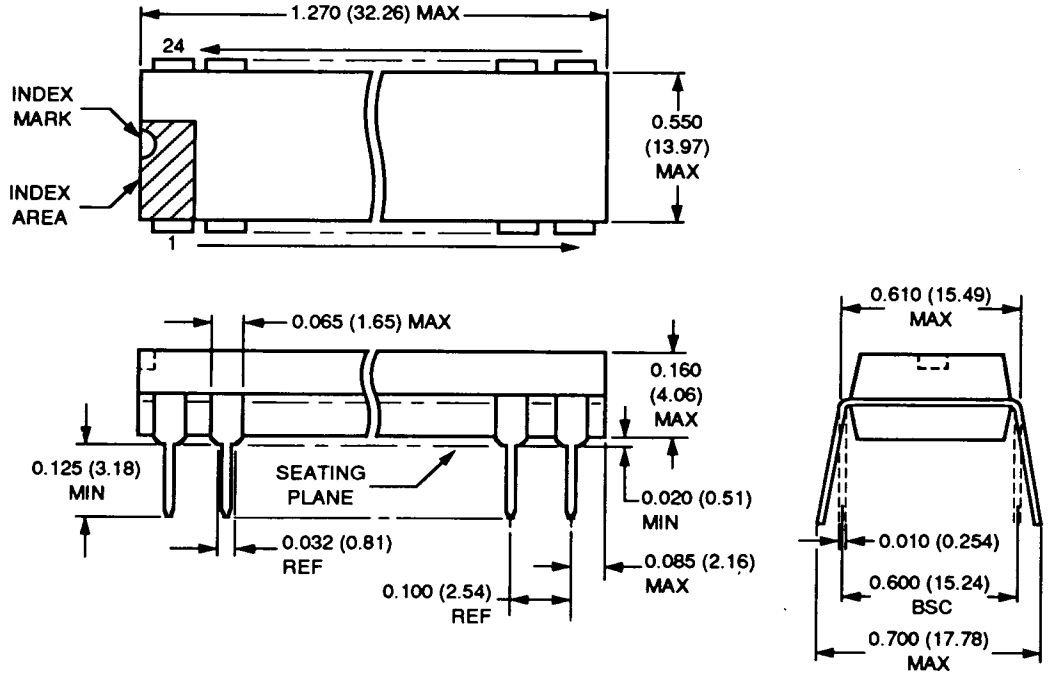


Figure 5. I/O Timing Diagram

Outline Diagrams

24-Pin, Plastic DIP

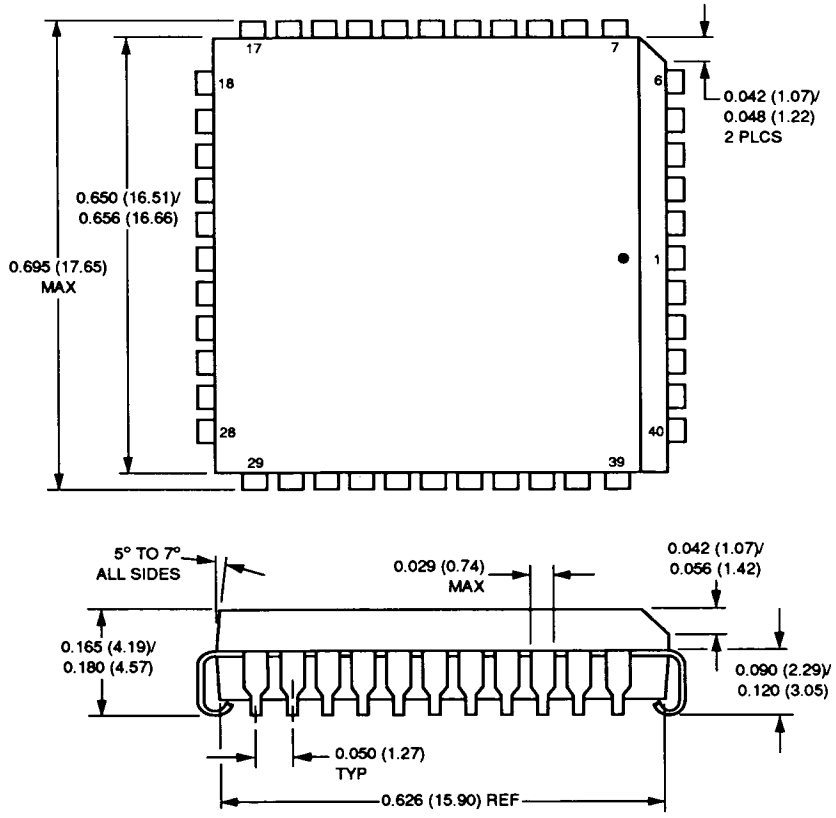
Dimensions are in inches and (millimeters).



Outline Diagrams (continued)

44-Pin PLCC

Dimensions are in inches and (millimeters).



Ordering Information

Device Code	Package	Temperature	Comcode
T7281-PC	24-Pin, Plastic DIP	0 °C to 70 °C	105587554
T7281-MC	44-Pin PLCC	0 °C to 70 °C	105587547

For additional information, contact your AT&T Account Manager or the following:
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